Electronic Version
Stylesheet Version v1.1.1

Description

DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY DEVICE

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a driving circuit of a liquid crystal display (LCD) device, and more particularly, to a driving circuit capable of reducing a difference between respective input voltages being input into driver integrated circuit (IC) chips.

[0003] 2. Description of the Prior Art

[0004] A thin film transistor display, such as a thin film transistor liquid crystal display (TFT-LCD), utilizes many thin film transistors, in conjunction with other elements such as capacitors and bonding pads, arranged in a matrix as switches for driving liquid crystal molecules to produce brilliant images. The advantages of the TFT-LCD over a conventional CRT monitor include better portability, lower

power consumption, and lower radiation. Therefore, the TFT-LCD is widely used in various portable products, such as notebooks, personal data assistants (PDA), electronic toys, etc. Gradually, the TFT-LCD is even replacing the CRT monitor in desktop computers.

[0005] Generally speaking, a TFT-LCD includes an upper substrate having a plurality of color filters, a lower substrate, and a plurality of liquid crystal molecules filled between the upper substrate and the lower substrate. Additionally, a plurality of scanning lines and a plurality of signal lines perpendicular to the scanning lines are formed on the lower substrate. At least one thin film transistor, used as a switch device of a pixel, is formed at an intersection of each of the scanning lines and each of the signal lines.

[0006] Please refer to Fig.1. Fig.1 is a schematic diagram of a liquid crystal display panel. As shown in Fig.1, a liquid crystal display panel 10 comprises a substrate 12 and an X-board 14. The X-board 14 is used for outputting signals into the substrate 12, for making the liquid crystal display panel 10 display an image. Moreover, the liquid crystal display panel 10 further comprises a plurality of tape carrier packages (TCP) 16 that are used for electrically connecting the X-board 14 and the substrate 12. Each of tape

carrier packages 16 packages a driver integrated circuit (IC) chip (not shown) thereon.

[0007] The substrate 12 comprises a plurality of scanning lines S_1-S_m, and a plurality of signal lines D_1-D_n perpendicular to the scanning lines S_1-S_m. A plurality of pixels (not shown) are therefore defined in an active region 18 by the scanning lines S_1-S_m and the signal lines D_1-D_n. Additionally, the substrate 12 further comprises an outer lead bonding (OLB) region 20, and a driving circuit 22 positioned in the outer lead bonding region 20. The driving circuit 22 includes driver IC chips 22a, 22b, and 22c that are used for outputting switching or addressing signals into the scanning lines S_1-S_m. The above-mentioned driver IC chips packaged in the tape carrier packages 16 are used for outputting image signals into the signal lines D_1-D_n.

[0008] Moreover, the driver IC chips 22a, 22b, 22c are directly formed on the substrate 12 by use of the chip-on-glass (COG) technology. The driving circuit 22 further comprises a plurality of conductive wires 24 for electrically connecting the driver IC chips 22a, 22b, and 22c. For reducing a production cost, the conductive wires 24 are directly formed on the substrate 12, which is so-called wiring on

array (WOA) technology. Thereafter, please refer to Fig.2. Fig.2 is an equivalent circuit of the driving circuit shown in Fig.1. As shown in Fig.2, an equivalent circuit 30 comprises the driver IC chips 22a, 22b, 22c, and resistors 32a, 32b. The resistor 32a connects the driver IC chips 22a and 22b, and corresponds to the conductive wires 24 located between the driver IC chips 22a and 22b as shown in Fig.1. Similarly, the resistor 32b is connected between the driver IC chips 22b and 22c, and corresponds to the conductive wires 24 located between the driver IC chips 22b and 22c as shown in Fig.1.

[0009] Referring to Fig.1, when the liquid crystal display panel 10 displays an image, a voltage pulse of a controlling signal 28 is output from the X-board 14, and then, the voltage pulse is sequentially inputted into the driver IC chips 22a, 22b, 22c through the tape carrier packages 16 and the conductive wires 24. Finally, switching or addressing signals are outputted from the driver IC chips 22a, 22b, 22c, and are inputted to the scanning lines S_1-S_m. However, due to the extremely large electrical resistance of the conductive wires 24, a voltage drop on each of the conductive wires 24 is significant. Therefore, when the voltage pulse of the controlling signal 28 is sequentially transmitted to

the driver IC chips 22a, 22b and 22c, the respective input voltages being input into the driver IC chips 22a, 22b and 22c are quite different. That is, the respective input voltages being input into the driver IC chips 22a, 22b and 22c vary with the positions of the driver IC chips 22a, 22b and 22c. In order to reduce the electrical resistance of the conductive wires 24, manufacturers currently usually increase a width or a thickness of the conductive wire 24.

[0010] Additionally, an insulation layer is formed between each of the scanning lines S_1-S_m and each of the signal lines D_1-D_n, and further, the scanning lines S_1-S_m and the signal lines D_1-D_n are made of conductive materials. Accordingly, a parasitic capacitor is formed at an overlapping region 26 of each of the scanning lines S_1-S_m and each of the signal lines D_1-D_n. As the voltage pulse input into each of the signal lines D_1-D_n is changed, the voltage variations on the signal lines D_1-D_n will be coupled to the scanning lines S_1-S_m through the parasitic capacitors at the overlapping regions 26, thus producing a glitch to disturb the controlling signal 28. That is, due to the parasitic capacitors at the overlapping regions 26, the voltage variations on the signal lines D_1-D_n will make the controlling signal 28 distort. Therein, the responding current (I)

of the controlling signal 28 versus time (t) comprises both of direct current (DC) and alternative current (AC), as shown in Fig.3. Unfortunately, the AC part of the responding current causes the respective input voltages being input into the driver IC chips 22a, 22b and 22c to be different. This causes the liquid crystal display panel 10 to display an image having band mura, and reduces a displaying quality of the liquid crystal display panel 10.

Summary of Invention

[0011] It is therefore a primary objective of the claimed invention to provide a driving circuit of a liquid crystal display (LCD) device to solve the above-mentioned problem.

[0012] According to the claimed invention,a driving circuit of a liquid crystal display device is provided. The driving circuit comprises a substrate, at least two driver integrated circuit (IC) chips positioned on the substrate, and an impedance device is electrically connected between the two driver IC chips for reducing a difference between respective input voltages being input into the two driver IC chips.

[0013] It is an advantage over the prior art that an impedance device including a capacitor and a resistor is utilized to connect the driver IC chips in the claimed invention. The

impedance device can reduce the equivalent impedance (Z) of the responding current of a controlling signal, so that the voltage drop on the impedance device can be reduced. Therefore, a difference between respective input voltages being input into the driver IC chips can be effectively decreased, and the driver IC chips can obtain approximately equal input voltages.

[0014] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment, which is illustrated in the multiple figures and drawings.

Brief Description of Drawings

[0015] Fig.1 is a schematic diagram of a liquid crystal display panel.

[0016] Fig.2 is an equivalent circuit of the driving circuit shown in Fig. 1.

[0017] Fig.3 is a relationship between the responding current of a controlling signal and the time.

[0018] Fig.4(A) is a schematic diagram of a driving circuit according to the present invention.

[0019] Fig.4(B) is an equivalent circuit of the driving circuit shown in Fig.4(A).

[0020] Fig.5 is a cross-sectional view along line 5-5" of Fig.4(A).

[0021] Fig.6(A) and Fig.6(B) are cross-sectional views along line 6-6" of Fig.4(A).

Detailed Description

[0022] Please refer to Fig.4(A). Fig.4(A) is a schematic diagram of a driving circuit according to the present invention. As shown in Fig.4(A), a liquid crystal display panel 40 comprises a substrate 42, and a driving circuit 44 positioned on the substrate 42. The driving circuit 44 at least comprises driver IC chips 46a, 46b, and metal wires 48a, 48b, 50. The driver IC chips 46a and 46b are directly formed on the substrate 42 by use of chip-on-glass (COG) technology, and are utilized for used for outputting switching or addressing signals to the scanning lines. The metal wires 48a, 48b, and 50 are utilized for connecting driver IC chips 46a and 46b. Additionally, the driving circuit 44 further comprises transparent conductive layers 52a and 52b. The transparent conductive layer 52a is positioned between the metal wires 48a, 50 and the driver IC chip 46a, while the transparent conductive layer 52b is connected between the metal wires 48b, 50 and the driver IC chip 46b. Furthermore, the electrical resistance of the

transparent conductive layer 52a and 52b can be modified to make each of the driver IC chips 46a and 46b obtain an equal input voltage. The electrical resistance of the transparent conductive layer 52a or 52b is determined by properly modifying a dimension of the transparent conductive layer 52a or 52b.

[0023] Please refer to Fig.4(B). Fig.4(B) is an equivalent circuit of the driving circuit shown in Fig.4(A). As shown in Fig.4(B), an equivalent circuit 60 comprises the driver IC chips 46a, 46b, and an impedance device 62 for connecting the driver IC chips 46a and 46b. The impedance device 62 comprises a capacitor 62a and a resistor 62b, which are electrically connected in parallel with each other. Moreover, the capacitor 62a is corresponding to the metal wires 48a and 48b shown in Fig.4(A), while the resistor 62b is corresponding to the metal wire 50 shown in Fig.4(A). In addition, the equivalent impedance (Z) of the impedance device 62 is represented by:

[0024] $Z=R/(1+j\omega RC)$ (1)

[0025] C is the capacitance of the capacitor 62a, R is the electrical resistance of the resistor 62b, j is an imaginary unit

$$j = \sqrt{-1}$$

, and ω is an angular frequency. As represented in Eq.1, when the angular frequency(ω) gets larger and larger, the equivalent impedance (Z) becomes smaller. That is, as the angular frequency(ω) of the electrical current passing through the impedance device 62 gets larger and larger, the equivalent impedance (Z) of the impedance device 62 becomes smaller.

[0026] As described above, there are parasitic capacitors existing between the scanning lines S_1-S_m and the signal lines D_1-D_n, so that the voltage variations on the signal lines D_1-D_n will be coupled to the scanning lines S_1-S_m through the parasitic capacitors at the overlapping regions 26, thus producing a glitch to disturb the controlling signal 28.Therefore, the responding current (I) of the controlling signal 28 versus time (t) comprises both of direct current (DC) and alternative current (AC), which leads to band mura. For reducing the influence of the above-mentioned disadvantages, the present invention utilizes the impedance device 62 including the capacitor 62a and resistor 62b to connect the driver IC chips 46a and 46b. The

impedance device 62 is used to eliminate the influence of the AC part of the responding current of the controlling signal 28 (or 54). Specifically, when the responding current flows through the impedance device 62, the capacitor 62a can reduce the equivalent impedance (Z) resulting from the AC part of the responding current. As the angular frequency (ω) of the AC part of the responding current of the controlling signal 28 (or 54) gets larger, the equivalent impedance (Z) of the impedance device 62 will become smaller. As a result, the voltage drop on the impedance device 62 can be reduced, and further, a difference between respective input voltages being input into the driver IC chips 46a and 46b is also decreased. Accordingly, the present invention can prevent the voltage variation on the signal lines from reducing a displaying quality of the liquid crystal display panel 40.

[0027] Please refer to Fig.5 to Fig.6(B). Fig.5 to Fig.6(B) are structural diagrams of the capacitor and the resistor according to the present invention. Furthermore, Fig.5 is a cross-sectional view along line 5-5" of Fig.4(A), while Fig.6(A) and Fig.6(B) are cross-sectional views along line 6-6" of Fig.4(A). As shown in Fig.5, the substrate 42 comprises the metal wires 48a and 48b thereon. An insulation layer

49 is located between the metal wires 48a and 48b, and a protective layer 51 is positioned on the metal wire 48a. The insulation layer 49 and the protective layer 51 are both composed of silicon nitride or silicon oxide. The metal wires 48a, 48b and the insulation layer 48 form a capacitor that is corresponding to the capacitor 62a shown in Fig.4(B).

[0028] Additionally, the substrate 42 further comprises the driver IC chips 46a, 46b, and the transparent conductive layers 52a, 52b thereon. The transparent conductive layer 52a is located between the driver IC chip 46a and the metal wire 48a. Furthermore, the metal wire 48a is connected to the transparent conductive layer 52a through a contact plug 53a, and the driver IC chip 46a is connected to the transparent conductive layer 52a through a gold bump 55a. Similarly, the transparent conductive layer 52b is located between the driver IC chip 46b and the metal wire 48b. The metal wire 48b is connected to the transparent conductive layer 52b through a contact plug 53b, and the driver IC chip 46b is connected to the transparent conductive layer 52b through a gold bump 55b. The transparent conductive layers 52a, 52b are composed of indium tin oxide (ITO), the metal wire 48b and the scanning

lines are simultaneously formed, and the metal wire 48a and the signal lines are concurrently formed.

[0029] As shown in Fig.6(A), the insulation layer 49 is located on the substrate 42, the metal wire 50 is formed on the insulation layer 49, and the protective layer 51 is formed on the metal wire 50. The insulation layer 49 and the protective layer 51 are both composed of silicon nitride or silicon oxide. The metal wire 50 is corresponding to the resistor 62b shown in Fig.4(B). Additionally, the substrate 42 further comprises the driver IC chips 46a, 46b, and the transparent conductive layers 52a, 52b thereon. The transparent conductive layer 52a is located between the driver IC chip 46a and the metal wire 50. Furthermore, the metal wire 50 is connected to the transparent conductive layer 52a through a contact plug 56a, and the driver IC chip 46a is connected to the transparent conductive layer 52a through a gold bump 55a. Similarly, the transparent conductive layer 52b is located between the driver IC chip 46b and the metal wire 50. The metal wire 50 is connected to the transparent conductive layer 52b through a contact plug 56b, and the driver IC chip 46b is connected to the transparent conductive layer 52b through a gold bump 55b. The transparent conductive layers 52a, 52b

are composed of indium tin oxide (ITO), the metal wire 50 and the scanning lines can be formed simultaneously, or the metal wire 50 can be formed concurrently with the signal lines.

[0030] Please refer to Fig.6(B). Fig.6(B) is a structural diagram of the resistor according to another embodiment of the present invention. As shown in Fig.6(B), the insulation layer 49 and the metal wire 50 are formed on the substrate 42, and the protective layer 51 is formed on the insulation layer 49 and the metal wire 50. The metal wire 50 includes metal wires 50a and 50b, and the insulation layer 49 is interposed between the metal wires 50a and 50b. The insulation layer 49 and the protective layer 51 are both composed of silicon nitride or silicon oxide. The metal wire 50 is corresponding to the resistor 62b shown in Fig.4(B).Additionally, the substrate 42 further comprises the driver IC chips 46a, 46b, and the transparent conductive layers 52a, 52b thereon. The metal wires 50a and 50b are respectively connected to the transparent conductive layer 52a through contact plugs 58a, and the driver IC chip 46a is connected to the transparent conductive layer 52a through a gold bump 55a. Similarly, the metal wires 50a and 50b are respectively connected to the transparent

conductive layer 52b through contact plugs 58b, and the driver IC chip 46b is connected to the transparent conductive layer 52b through a gold bump 55b. The transparent conductive layers 52a, 52b are composed of indium tin oxide (ITO), the metal wire 50b can be formed simultaneously with the scanning lines, and the metal wire 50a and the signal lines can be formed simultaneously.

[0031] The above-mentioned driving circuit is used to output switching or addressing signals to the scanning lines. Moreover, the driving circuit of the present invention can be used to output image signals to the signal lines, as is known to those skilled in the art.

[0032] Compared to the prior art, an impedance device including a capacitor and a resistor is utilized to connect the driver IC chips in the present invention. When the voltage variation on the signal lines causes the responding current of the controlling signal to generate alternative current and direct current, the impedance device can reduce the equivalent impedance (Z) of the responding current of the controlling signal. The voltage drop on the impedance device can be reduced, so that a difference between respective input voltages being input into the driver IC chips can be effectively decreased, and the driver IC chips can ob-

tain approximately equal input voltages. As a result, the present invention can prevent the voltage variation on the signal lines from reducing a displaying quality of the liquid crystal display panel.

[0033] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bound of the appended claims.